QUARTERLY TECHNICAL REPORT
28 July 2005 to 27 October 2005
NREL Subcontract ZXL-5-44205-11
Principal Investigator: J. David Cohen
Organization: University of Oregon

We report results of our research activities under NREL Subcontract ZXL-5-44205-11 during the second quarter of Phase I. For the current Subcontract under the Thin-Film Partnership program, our Statement of Work indicated that we would devote roughly 30% of our effort to CIS thin-film photovoltaics, and 70% to silicon-based thin film technologies. Thus, this Quarterly will be devoted to reporting the some of our results obtained studying CIGS cells. Our stated goal in our CIGS work is to apply our measurement techniques to try to understand differences between the best laboratory cells, and those fabricated using processes better suited for manufacturing. To begin, we have been examining laboratory CIGS devices with high levels of performance (Task 1.4). This report will document what we have learned from a set of high performance NREL CIGS devices that were obtained in July, 2005, from Miguel Contreras.

Rather than characterizing only the best NREL CIGS devices, we thought it would be much more interesting to compare the results of our measurements on NREL devices with varying levels of performance. In that manner, we might be able to identify differences that might be correlated with those variations in performance. We therefore obtained three samples, each containing 6 devices, with average efficiencies in the 14-15% range (C1919-11), in the 16-17% range (C1818-21), and in the 17-18% range (C1924-1). Among the total of 18 devices, 4 or 5 seemed anomalous (primarily because of low shunt resistances) and we selected 8 of the remaining devices for detailed study that seemed to represent a good range of performance parameters. The performance parameters of the 8 devices we chose to characterize in detail, using admittance, DLCP profiling, and CV profiling, are listed in Table I.

Some useful insight into the performance parameters of these 8 samples may be obtained by the plots displayed in Fig. 1 and 2. In Figure 1 we examine the relationship between the open

TABLE I. NREL devices from 3 depositions chosen for detailed characterization using our experimental methods. The area of each sample device was 0.406 cm^2.

Device Number	V_{OC} (volts)	J_{SC} (mA/cm^2)	Fill Factor (%)	Efficiency (%)
C1919-11 Cell 3	0.630	32.95	71.43	14.833
C1919-11 Cell 4	0.642	32.51	68.99	14.393
C1813-21 Cell 3	0.657	33.26	76.08	16.613
C1813-21 Cell 4	0.664	32.67	77.82	16.888
C1813-21 Cell 6	0.667	33.19	77.52	17.168
C1924-1 Cell 4	0.724	30.82	78.19	17.449
C1924-1 Cell 5	0.717	30.81	77.44	17.118
C1924-1 Cell 6	0.714	30.95	77.07	17.039

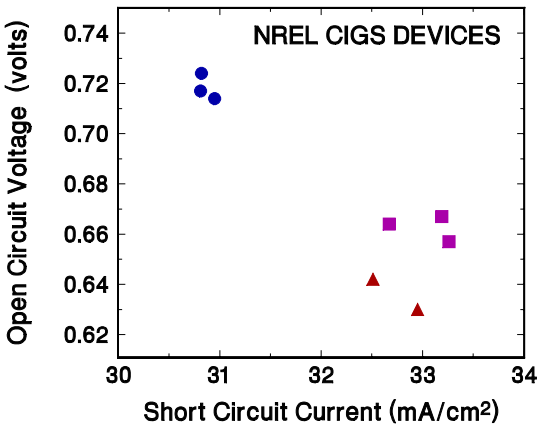

FIG. 1. Open circuit voltage vs. short circuit current for the 8 devices listed in Table I: ▲ for the C1919 devices, ■ for the C1813 devices, and ● for the C1924 devices.

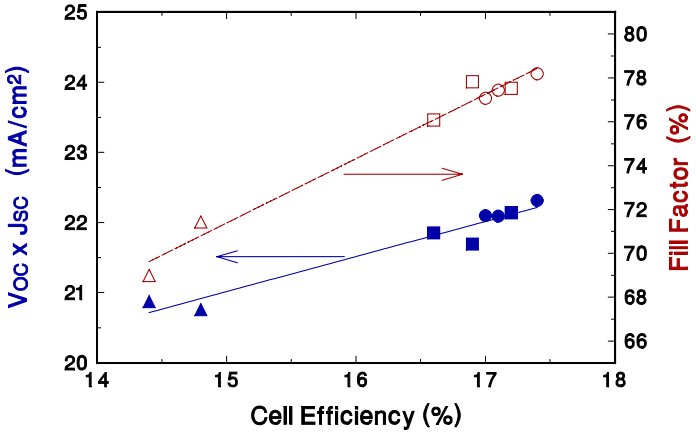

FIG. 2. Relationship of V_{OC}-J_{SC} products and Fill Factors to overall device efficiencies. This seems to indicate a dominant role for the Fill Factors in the overall device performance. The symbols shapes are used in the same manner as in Fig. 1.

circuit voltage and short circuit current, while in Figure 2 we examine the relation between the device efficiency and both the Fill Factor and the V_{OC}-J_{SC} product. Figure 1 indicates that the 3 devices from sample C1924-1 are somehow distinctly different from the other 5 devices in that they have significantly higher values of V_{OC} and lower values of J_{SC}. This might indicate, for example, that the absorber in C1924-1 contained a higher fraction of Ga than did samples C1813-21 or C1919-11. Figure 2 indicates that the variation in efficiencies for these 8 devices is correlates most strongly with Fill Factor, but that the V_{OC}-J_{SC} product increases monotonically with device efficiency as well. There were no obvious correlations between device efficiencies and either the open-circuit voltage or short-circuit currents for this set of samples.

All of the measurements to characterize the electronic properties of these devices were carried out by my graduate student Peter Erslev. In Figure 3 I display a subset of his representative results from admittance spectroscopy for these devices; specifically, for one device from each deposition. Except possibly for the C1919-11 device, these devices show very little evidence for the admittance step typical of devices from other laboratories. There does appear to be a roll-off at the very highest frequencies for the other 2 devices; however, this does not correspond to the deep acceptor admittance feature that is normally seen. Rather, this roll-off is more likely due either to impedance problems with our current preamplifier or, possibly, due to the limited conductance of the window layer. Both issues arise because these devices have much larger areas than those we have measured in the past. For example, a limited sheet conductance would reduce the effective area of the sample at higher frequencies and low temperatures and produce the type of decrease in capacitance that is observed.

The lack of a distinct admittance "deep acceptor" step for the highest efficiency CIGS devices is well known, particularly from the results of a CIS Thin-Film Team collaboration.[1] We and our Colorado State collaborators also previously pointed out the lack of such a "deep acceptor" feature in the admittance spectra of NREL devices in a recent paper comparing NREL and SSI CIGS devices.[2] However, in spite of the lack of such a feature in these admittance spectra, and the lack of even any major differences in the junction capacitances, the efficiencies of the devices varies considerably, as seen in Table I. Hopefully, then, we can observe more pronounced differences from our other types of characterization measurements.

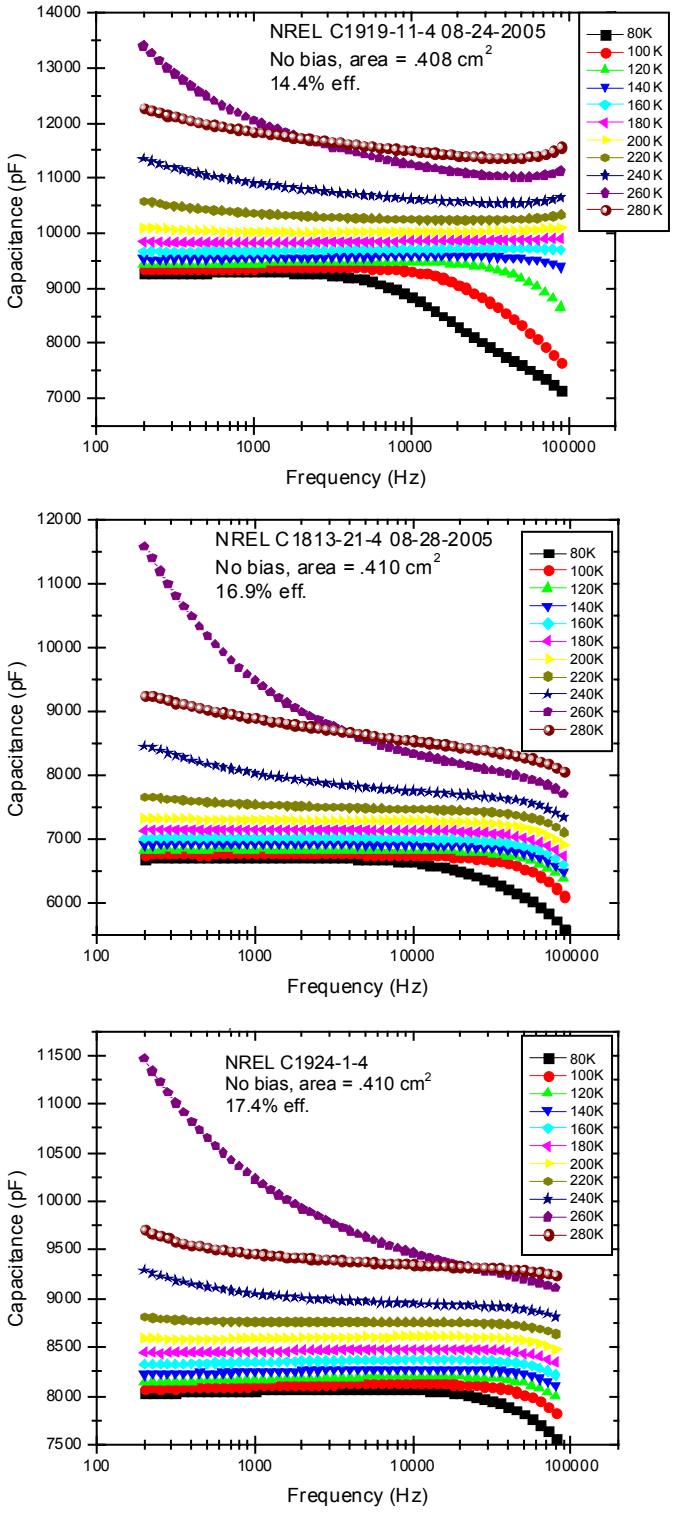

FIG. 3. Admittance spectra at zero applied bias for one device from each of the 3 sample depositions. The spectra from neither the C1813-21 device nor the C1924-1 device exhibit the typical admittance step due the response from the deep acceptor level observed in devices from most other laboratiories. The low temperature falloff at high frequency for these two devices is believed to be a measurement artifact (see discussion in text). Note that the depletion capacitance varies slightly from sample to sample, but does not correlate in any obvious manner to the device cell performance.

In Figure 4 we display results of both DLCP and standard CV profiling for these same 3 representative sample devices. The sample bias was varied from 1 volt reverse to +0.4 volts forward and, in all cases, we observe quite a pronounced spatial variation in these profiles. The temperature dependence is quite interesting: For temperatures below about 160K the profiles are

nearly temperature independent, and the differences between the DLCP and CV curves are very minor. This changes for the profiles obtained at 200K and above. Indeed, for the 280K profiles, the differences between the DLCP and CV profiles become quite pronounced, with the latter showing a dramatic peak in some cases.

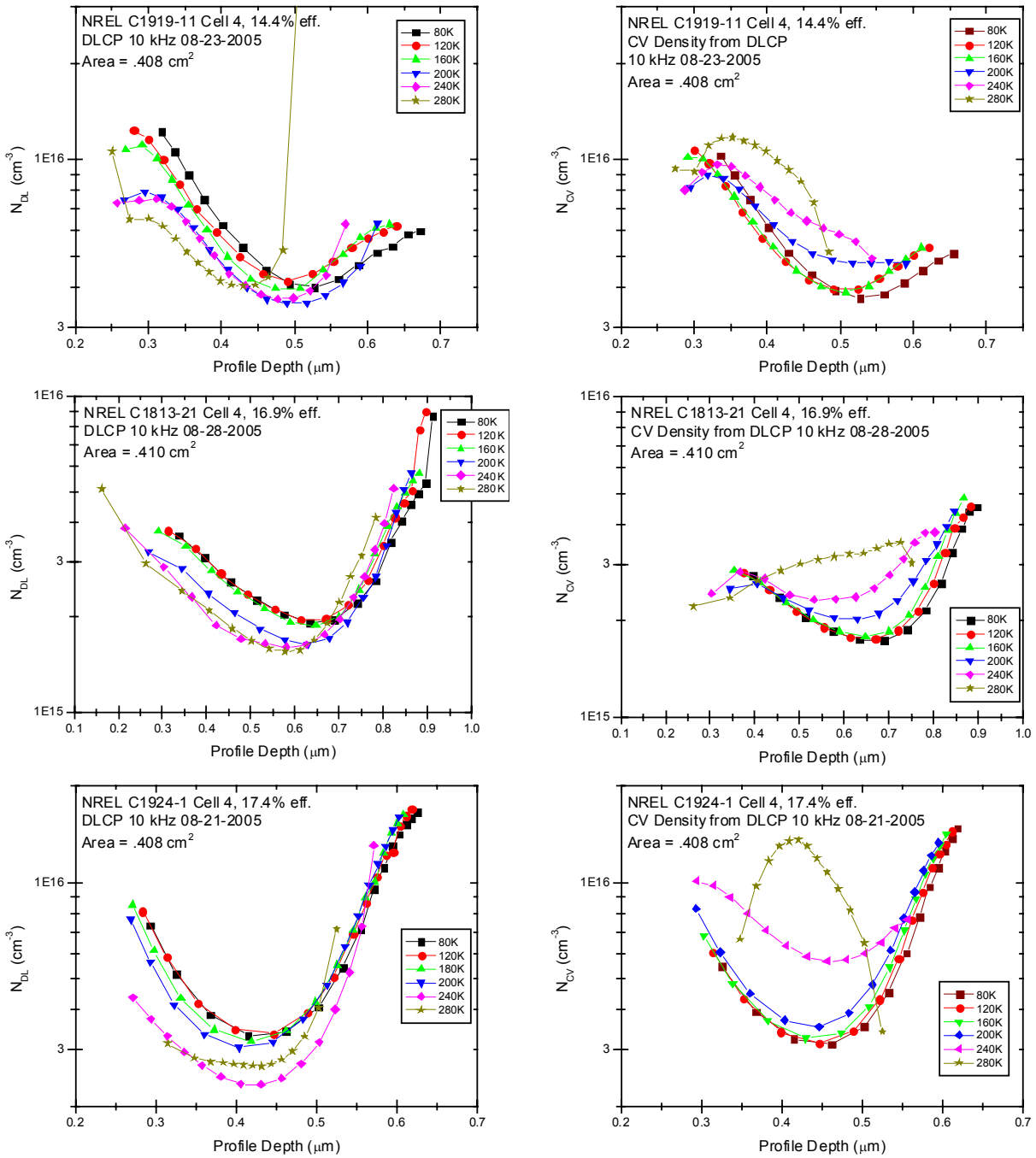

FIG. 4. Drive-level capacitance profiles (DLCP) and CV profiles for representative devices over a broad range of temperatures. These data were taken using DC biases that varied from –1V to +0.4V, in 0.1V increments. Note the strong spatial variation in these profiles in all cases. Also note the similarity between the DLCP and CV profiles for temperatures of 160K and below, but the marked differences for the highest temperatures employed.

Because of the observed large spatial variations in these profiles, the usual simple interpretation of DLCP in terms of the expression [3]

$$N_{DL}(x) = p + \int_{E_F^0}^{E_V+E_e} g(E,x)dE \qquad \text{with } E_e = k_B T \log(\nu/2\pi f) \tag{1}$$

to obtain information about the defect state distribution may not be very accurate. However, we have recently enhanced some of our numerical modeling programs so that we can extract more detailed information from the types of DLCP and CV profiles shown. This analysis has just begun, however, so that we cannot present results from our more accurate analysis in this Report.

Nonetheless, we can offer some general conclusions at this time. First of all, the large CV profile densities at high temperature are almost certainly due to very deep defects near the barrier interface (even though they occur for profile "distances" that appear to be at some distance from the barrier). In this case, a clearer picture of the distribution of these deep, near interface states must await a more detailed numerical modeling analysis. For this reason we will concentrate our remaining comments on our DLCP results. Clearly, the appearance of the DLCP profiles is qualitatively different for the different representative samples. For the C1919 (lowest performance) device, the DLCP profile is high in the region near the barrier interface (obtained under forward bias so that this region lies in the high field region under normal operation), and relatively low at larger distances from the barrier (this is the region that lies outside the depletion region in nearly zero field). For the other two, higher performance devices the DLCP density is relatively lower in the normally depleted region close to the barrier, and relatively higher in the zero-field region at larger distances.

To get a better idea of how our DLCP results might be correlated with the device performance, we have plotted in Figure 5 how the device efficiencies vary with the DLCP densities in the normally depleted region of the device closer to the barrier interface [Fig. 5(a)] and also with the DLCP density in the normally zero-field region of the absorber farther away from the barrier interface [Fig. 5(b)].

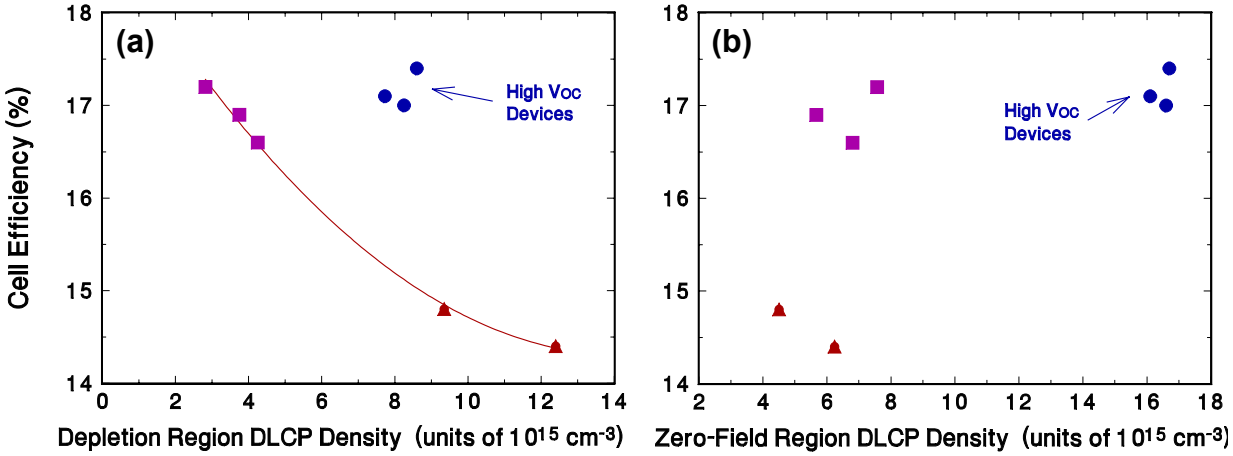

FIG. 5. Correlation of device efficiencies with the DLCP determined densities in the **(a)** depletion region near the barrier interface, and **(b)** the zero field region of the absorber farther from the barrier interface. The symbols are used in the same manner as in Figs. 1 and 2; namely: ▲ for the C1919 devices, ■ for the C1813 devices, and ● for the C1924 devices. These latter devices were found to have significantly higher values of V_{OC} than the others, and are so labeled.

From Fig. 5(a) we see that, for the 5 devices from two of the depositions, there appears to be quite a good inverse correlation between the cell efficiencies and the DLCP densities close to the barrier interface. It is thus tempting to connect the larger DLCP densities in the depletion region of these devices with a larger concentration of recombination centers that lower the fill factor, and hence the efficiencies. On the other hand, the cells from the third, C1924-1, deposition do not follow this trend. However, we believe that this might be the result of our inaccurate interpretation of these DLCP profiles since, for the C1924 devices (see Fig. 4), they exhibit the largest spatial variations and thus may be less likely to reflect the true spatial distributions in the electronic properties. Indeed, we note that some of our recent modeling has indicated that the type of large upturn in the DLCP profiles that are exhibited for the C1924 devices at forward bias probably reflect characteristics of the barrier interface itself, rather than defects within the absorber. In contrast, the DLCP curves for the C1919 and C1813 devices appear show signs of flattening out at small profile distances. In some of our attempts to model similar kinds profiles in more detail, we have found that they usually reflect the actual defect densities within the absorber layer close to the barrier interface.

Fig. 5(b) indicates that the high V_{OC} devices are also distinctive in displaying much higher DLCP densities in the zero-field region outside the depleted part of the absorber. This is undoubtedly beneficial for the device performance for two reasons: (1) It means that the hole carrier density is higher in this region, leading to a lower resistivity within the part of the absorber less active in power generation, and (2) The higher DLCP density reflects a hole carrier density that is higher by a factor of 2.5 to 4 times that of the five less efficient devices. This means that the hole Fermi level near the back contact is probably 25-35 meV closer to E_V, and this will be reflected in a higher value of V_{OC}. We believe that this could account for about half of the difference in V_{OC} for the C1924-1 devices compared to the other devices. The remainder of the difference in V_{OC}, we believe, likely comes from differences in the composition profiles of the C1924-1 devices.

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